REMARKS

Claims 1-22, as amended, remain herein. Claims 23-52 remain herein but are presently withdrawn from consideration.

Applicants appreciate the statements in the Office Action that claims 4, 6-11, 15 and 17-22 would be allowable if rewritten in independent form including all of the limitations of the independent claim(s) from which they depend. As explained herein, applicants believe that all claims 1-22 are now in condition for allowance.

Minor, editorial changes have been made in claims 1-22.

The specification has been edited to correct a minor formality.

1. Claims 1, 2, 12 and 13 were rejected under 35 U.S.C. §102(b) over Goel U.S. Patent 4,204,633.

The presently claimed fault detecting method comprises providing a fault list corresponding to (a) information identifying physical sites of a semiconductor integrated circuit where a possible fault is likely to occur or (b) information required to reduce faults, and detecting faults in a

semiconductor integrated circuit to which said fault list corresponds by using the fault list. This method is nowhere disclosed or suggested in the cited reference.

The Office Action cites Goel '633, column 6, lines 3-5, as allegedly disclosing that each selected fault from a fault list is a fault associated with a specific node of the Goel '633 combinational or sequential circuit logic network, and on that basis the Office Action suggests that such description allegedly corresponds to applicants' detecting faults based on a fault list corresponding to information identifying sites of a semiconductor integrated circuit where a fault is likely to occur, or corresponding to information required to reduce faults. Actually, Goel '633, column 6, lines 3-5, discloses "[e]ach selected fault may be at a 'stuck-high binary level 1 or a 'stuck-low' binary level 0 at a particular node of the network." Thus, while Goel '633 discloses that each selected fault may be at a 'stuck-high binary level 1 or a 'stuck-low' binary level 0 at a particular node of the network, Goel '633 does not suggest (1) that such selected fault corresponds to either information identifying physical sites of a semiconductor

integrated circuit where a fault is likely to occur, or information required to reduce faults, and (2) detecting faults in the integrated circuit by using the fault list, as recited in applicants' claims 1 and 12.

Moreover, Goel '633, column 5, line 65, to column 6, line 5, discloses feeding "network topology" and the designer's selection of a set of faults to be tested, as two possible inputs to a test pattern generator. "Network topology" refers to a schematic representation of connections in a network and does not refer to an actual physical layout of such network. Therefore Goel '633 does not provide a fault list corresponding to information identifying physical sites of an integrated circuit or detect faults in the semiconductor integrated circuit by using the fault list, as recited in applicants' claims 1 and 12.

For the foregoing reasons, Goel '633 fails to disclose all elements of applicants' claimed invention, and therefore is not a proper basis for rejection under §102. And, there is no disclosure or teaching in Goel '633 that would have suggested the desirability of modifying any portions thereof effectively

to anticipate or suggest applicants' presently claimed invention. Claim 2, which depends from claim 1, is allowable for the same reasons described herein for claim 1, and claim 13, which depends from claim 12, is allowable for the same reasons described herein for claim 12. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

8. Claims 3, 5, 14 and 16 were rejected under 35 U.S.C. §103(a) over Goel '633, and Satoshi et al. U.S. Patent 5,587,930.

Claims 2 and 5, which depend from claim 1, are allowable for the same reasons described herein for claim 1, and claims 14 and 16, which depend from claim 12, are allowable for the same reasons described herein for claim 12.

All claims 1-22 are now proper in form and patentably distinguished over all grounds of rejection cited in the Office Action. Accordingly, allowance of all claims 1-22 is respectfully requested.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

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Date

Roger W. Parkhurst
Registration No. 25,177
Robert N. Wieland
Registration No. 40,225

RWP:RNW/mhs

Attorney Docket No.: YMOR:186

PARKHURST & WENDEL, L.L.P.
1421 Prince Street, Suite 210
Alexandria, Virginia 22314-2805
Telephone: (703) 739-0220